REMARKS

Claims 7-11 were examined. No claims are amended or added. Claims 7-11 remain in the application.

The Patent Office rejects claims 7-11 35 under U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,879,988 of Chen, et al. (Chen). Chen teaches a stacked capacitor for a DRAM cell. Referring to Figures 2-9 referencing the prior art, Chen describes a storage electrode having three fin-shaped parts of doped (i.e., conductive) polysilicon layers 15, 17 and 19 with a dielectric film 20 covering the doped polysilicon layers and a doped polysilicon layer 21 formed as a plate electrode. *See* col. 2, line 60 - col. 3, line 8. To form the fin-shaped parts, Chen describes alternately depositing silicon dioxide layers and the doped poly layers on a silicon substrate and removing the silicon dioxide layers. Thus at one point, Chen teaches SiO_2 layer 14 over Si_3N_4 layer 13.

Independent claim 7 is not anticipated by Chen, because Chen does not describe a method including forming an interlayer dielectric comprising alternating layers of dissimilar dielectric materials in a multilayer stack over a metal layer of a device structure. Chen forms its stacked capacitor over silicon substrate not a metal layer. Claim 7 is also not anticipated by Chen, because Chen does not describe having a via having a corrugated sidewall. With reference to Figures 2-9 there is no description or illustration of a via having a corrugated sidewall.

Chen further does not describe forming a decoupling capacitor stack in the via that conforms to the sidewall of the via. As noted, Chen does not describe a corrugated sidewall and therefore does not describe a decoupling capacitor stack in the via that conforms to the sidewall of the via.

Claims 8-11 depend from claim 7 and therefore contain all the limitations of that claim. For at least the reasons stated with respect to claim 7, claims 8-11 are not anticipated by Chen.

Applicant respectfully requests that the Patent Office withdraw the rejection of claims 7-11 under 35 U.S.C. § 102(b).

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, VA 22313-1450.

Suzanne Johnston 12/18/06
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